THAT WHICH IS CLAIMED IS:

1. An improved voltage translator for digital electronic circuits providing reduced rise times, fall times and transition times that remain independent of operating conditions, comprising:

a first high-voltage switch driven by the input low-voltage signal;

a second high-voltage switch driven by the complement of the input low-voltage signal, in which (a) the output of the first high-voltage switch enabling an active switched load connected to the output of the second high-voltage switch when the first high-voltage switch is OFF and disabling it when the first high-voltage switch is ON, (b) the output of the second high-voltage switch enabling an active switched load connected to the output of the first high-voltage switch when the second high-voltage switch is OFF and disabling it when the second high-voltage switch is ON, and (c) the output from the low-to-high voltage translator being provided by the output from the second high-voltage switch;

a switched active pull-up at the output of the first high-voltage switch, controlled by the input low-voltage signal and gated by the output from the low-to-high-voltage translator; and

a switched active pull-down at the output of the first high-voltage switch, controlled by the input low-voltage signal and gated by the complement of the output from the low-to-high-voltage translator, so at to provide regenerative pull-up and pull-down that also counteracts the bootstrap capacitance at the output of the first high-voltage switch.

2. A method for providing voltage translation for digital electronic circuits enabling reduced rise times, fall times and transition times that remain independent of operating conditions, comprising the steps of :

providing a first high-voltage switch driven by the input low-voltage signal;

providing a second high-voltage switch driven by the complement of the input low-voltage signal;

causing the output of the first high-voltage switch to enable an active switched load connected to the output of the second high-voltage switch when the first high-voltage switch is OFF and disable it when the first high-voltage switch is ON;

causing the output of the second high-voltage switch to enable an active switched load connected to the output of the first high-voltage switch when the second high-voltage switch is OFF and disable it when the second high-voltage switch is ON;

providing the output from the low-to-high voltage translator from the output from the second high-voltage switch; and

providing a switched active pull-up at the output of the first high-voltage switch, controlled by the input low-voltage signal and gated by the output from the low-to-high-voltage translator and a switched active pull-down at the output of the first high-voltage switch, controlled by the input low-voltage signal and gated by the complement of the output from the low-to-high-voltage translator, so as to provide regenerative pull-up and pull-down that also counteracts the bootstrap capacitance at the output of the first high-voltage switch.

3. A voltage translator circuit comprising:

a first circuit portion including a load coupled to a high voltage power supply, an intermediate node, and an output;

a second circuit portion including bias circuitry coupled to the intermediate node, the output, and ground;

a third circuit portion including a switch coupled to a low voltage power supply, an input, the output, and the intermediate node; and

a fourth circuit portion including a switch coupled to the input, the intermediate node, the output, and ground.

4. A voltage translator circuit as in claim 3 in which the first circuit portion comprises a pair of cross-coupled PMOS transistors.

5. A voltage translator circuit as in 3 in which the second circuit portion comprises a pair of NMOS transistors.

6. A voltage translator circuit as in claim 3 in which the second circuit portion comprises a pair of NMOS transistors.

7. A voltage translator circuit as in claim 3 in which the second circuit portion comprises a pair of NMOS transistors having gates coupled through an inverter.

8. A voltage translator circuit as in 3 in which the third circuit portion comprises a PMOS transistor and an NMOS transistor.

9. A voltage translator circuit as in claim 3 in which the third circuit portion comprises a serially-coupled PMOS transistor and an NMOS transistor.

10. A voltage translator circuit as in claim 3 in which the fourth circuit portion comprises first and second serially-coupled NMOS transistors, wherein the gate of the second NMOS transistor is coupled to the output via an inverter.